WHAT IS CLAIMED IS:

1. A chip to chip interface comprising:

a driver configured to provide a first signal in response to a change in first data at one edge of a clock signal and a second signal in response to a change in second data at another edge of the clock signal; and

a receiver configured to receive the first signal and the second signal and toggle a first bit in response to the first signal and toggle a second bit in response to the second signal.

2. The chip to chip interface of claim 1, wherein the receiver is configured to provide the first bit to represent the first data and to provide the second bit to represent the second data.

3. The chip to chip interface of claim 1, wherein the first data is positive edge data in a double data rate data stream.

4. The chip to chip interface of claim 1, wherein the second data is negative edge data in a double data rate data stream.

5. The chip to chip interface of claim 1, wherein the receiver is configured to provide the first bit to a circuit at each positive edge of the clock signal.

6. The chip to chip interface of claim 1, wherein the receiver is configured to provide the second bit to a circuit at each negative edge of the clock signal.

7. The chip to chip interface of claim 1, wherein the first signal is a high voltage pulse.

8. The chip to chip interface of claim 1, wherein the second signal is a low voltage pulse.

9. The chip to chip interface of claim 1, wherein the driver is configured to provide the first signal in one portion of the clock signal and the second signal in another portion of the clock signal.

10. The chip to chip interface of claim 9, wherein the one portion is one half cycle of the clock signal and the second portion is another half cycle of the clock signal.

11. The chip to chip interface of claim 1, wherein the driver is configured to compare current first data to previous first data and supply the first signal in response to a difference between the current first data and the previous first data.

12. The chip to chip interface of claim 11, wherein the previous first data is supplied one clock cycle before the current first data.

13. A memory interface comprising:

a memory controller comprising a driver configured to provide a first signal in response to a change in first data at positive edges of a clock signal and a second signal in response to a change in second data at negative edges of the clock signal.

14. The memory interface of claim 13, further comprising:

a memory comprising a receiver configured to receive the first signal and the second signal and toggle a first bit in response to the first signal and toggle a second bit in response to the second signal.

15. A chip to chip communication bus comprising:

a driver configured to receive a double data rate data signal and provide a high voltage pulse in response to a change in positive edge data and to provide a low voltage pulse in response to a change in negative edge data; and

a receiver configured to receive the high voltage pulse and the low voltage pulse and toggle a first bit in response to the high voltage pulse and toggle a second bit in response to the low voltage pulse.

16. The chip to chip communication bus of claim 15, wherein the receiver is configured to provide the first bit at the rising edge of the clock signal and the second bit at the negative edge of the clock signal to recreate the double data rate data signal.

17. The chip to chip communication bus of claim 15, wherein the double data rate data signal is a 3.2 GHz double data rate data signal.

18. The chip to chip communication bus of claim 15, wherein the double data rate data signal is a 1.6 GHz double data rate data signal.

19. The chip to chip communication bus of claim 15, wherein the receiver comprises a first comparator configured to toggle the first bit and a second comparator configured to toggle the second bit.

20. The chip to chip communication bus of claim 19, wherein the first comparator receives a first reference signal to compare to the high voltage pulse and the second comparator receives a second reference signal to compare to the low voltage pulse.

21. The chip to chip communication bus of claim 20, wherein the first reference signal comprises a first constant voltage and the second reference signal comprises a second constant voltage.

22. The chip to chip communication bus of claim 20, wherein the first reference signal and the second reference signal comprise sinusoidal signals.

23. A chip to chip interface comprising:

means for providing a first signal in response to a change in even data in a double data rate data stream;

means for providing a second signal in response to a change in odd data in a double data rate data stream;

means for receiving the first signal and toggling a first bit in response to the first signal; and

means for receiving the second signal and toggling a second bit in response to the second signal.

24. The chip to chip interface of claim 23, wherein the means for providing the first signal comprises means for providing the first signal by masking a clock signal in response to no change in the even data in the double data rate data stream.

25. The chip to chip interface of claim 23, wherein the means for receiving the first signal comprises means for latching the first bit with a clock signal.

26. A method for communicating data between chips comprising:

generating a first signal in a first chip in response to a change in first data at positive edges of a clock signal;

generating a second signal in the first chip in response to a change in second data at negative edges of the clock signal;

passing the first signal and the second signal from the first chip to a second chip;

toggling a first bit in the second chip in response to the first signal; and

toggling a second bit in the second chip in response to the second signal.

27. The method of claim 26, wherein passing the first signal and the second signal from the first chip to the second chip comprises passing the first signal

and the second signal from the first chip to the second chip through a single signal path.

28. The method of claim 26, wherein generating the first signal comprises masking the clock signal to provide a logic high pulse.

29. The method of claim 26, wherein generating the second signal comprises masking the clock signal to provide a logic low pulse.

30. The method of claim 26, comprising setting the first bit and the second bit to initial values.

31. The method of claim 26, comprising providing the first bit to a circuit in the second chip on each rising edge of the clock signal and providing the second bit to the circuit on each falling edge of the clock signal.